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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,995	11/30/2001	Giovanni Frezza	856063.722	3898

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/997,995	FREZZA, GIOVANNI	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19,21,22,24,25,27-33 and 36-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,21,22,24,25,27-33 and 36-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 25, 28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,823,605 to Stein.

Regarding claim 25, Stein (figure 1) teaches a packaged electronic device ready for electronic use, comprising:

a semiconductor integrated electronic circuit (1);

a plastic protective package (3) surrounding and supporting the electronic circuit (1), the protective package (3) having a window (6) over a portion of the electronic device such that the electronic device can be activated from outside of the protective package (3); and

an elastic protective layer (5) positioned in the window (6), the protective layer (5) being structured to enable the electronic device to be activated through the protective layer when the electronic device is in use (column 2, lines 10-45).

a membrane (4) positioned between the electronic circuit (1) and the protective layer (5), the membrane (4) having a concave surface facing the electronic circuit (1) so as to leave a recess (9) between the concave surface and the electronic circuit.

Regarding claim 28, Stein teaches the window (6) has walls tapering toward the electronic circuit (1).

Regarding claim 30, Stein teaches the electronic circuit (1) includes a pressure sensor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19, 21, 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,948,991 to Nomura et al. in view of US Patent No. 4,894,707 to Yamawaki et al.

Regarding claim 19, Nomura et al. (figure 6) teach a packaged electronic device ready for electronic use, comprising:

a semiconductor integrated electronic circuit (130);

a plastic protective package (122) surrounding and supporting the electronic circuit (130), the protective package (122) having a window (127) over a portion of the electronic device (130) such that the electronic device can be at least partially activated from outside of the protective package (122); and

a projecting portion of elastic material (132) projecting from a surface of the electronic device (130) into the window (127).

It is inherent that the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use because a pressure sensitive diaphragm always receives pressure from the top surface of the diaphragm.

Nomura et al. differ from the claimed invention by not showing the projecting portion is shaped to form a ring on the electronic circuit. However, Yamawaki et al. (figures 1A-2G) teach the projecting portion is shaped to form a ring (3) on the chip (1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yamawaki et al. into the device taught by Nomura et al. because it prevents the contact of mold to the electronic device. The combined device shows the projecting portion is shaped to form a ring on the electronic circuit.

Regarding claim 21, Nomura et al. teach the window (127) has tapering walls toward the electronic circuit (130).

Regarding claim 24, Nomura et al. teach the electronic circuit includes a pressure sensor.

Regarding claim 27, Nomura et al. (figure 6) teach a packaged electronic device ready for electronic use, comprising:

a semiconductor integrated electronic circuit (130);

a plastic protective package (122) surrounding and supporting the electronic circuit (130), the protective package (122) having a window (127) over a portion of the electronic device such that the electronic device can be activated from outside of the protective package (122); and

an elastic protective layer (132) positioned in the window (127).

It is inherent that the protective layer being structured to enable the electronic device to be activated through the protective layer when the electronic device is in use because a pressure sensitive diaphragm always receives pressure from the top surface of the diaphragm.

Nomura et al. differ from the claimed invention by not showing the protective layer is shaped to form a ring on the electronic circuit. However, Yamawaki et al. (figures 1A-2G) teach the projecting portion is shaped to form a ring (3) on the chip (1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yamawaki et al. into the device taught by Nomura et al. because it prevents the contact of mold to the electronic device. The combined device shows the protective layer is shaped to form a ring on the electronic circuit.

5. Claims 22, 29, 31-33, 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,894,707 to Yamawaki et al. in view of US Patent No. 5,948,991 to Nomura et al.

Regarding claim 22,Yamawaki et al. (figures 1A-2G) teach a packaged electronic device ready for electronic use, comprising:

a semiconductor integrated electronic circuit (1);

a plastic protective package (9) surrounding and supporting the electronic circuit (1), the protective package (9) having a window over a portion of the electronic device (1) such that the electronic device can be at least partially activated from outside of the protective package (9).

Yamawaki et al. differ from the claimed invention by not showing a projecting portion of elastic material projecting from a surface of the electronic device into the window, the projecting

portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use, wherein the projecting portion is surrounded by dyke formed on a surface of the electronic circuit. However, Nomura et al. (figure 6) teach a projecting portion of elastic material (132) projecting from a surface of the electronic device (130) into the window (127). Nomura et al. inherent teach the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use because a pressure sensitive diaphragm always receives pressure from the top surface of the diaphragm. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate teaching of Nomura et al. into the device taught by Yamawaki et al. because it protects the sensor chip from the external damage. The combined device shows a projecting portion of elastic material projecting from a surface of the electronic device into the window, the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use, wherein the projecting portion is surrounded by dyke formed on a surface of the electronic circuit.

Regarding claim 29, Yamawaki et al. (figures 1A-2G) teach a packaged electronic device ready for electronic use, comprising:

a semiconductor integrated electronic circuit (1);

a plastic protective package (9) surrounding and supporting the electronic circuit (1), the protective package (9) having a window over a portion of the electronic device (1) such that the electronic device can be at least partially activated from outside of the protective package (9).

Yamawaki et al. differ from the claimed invention by not showing an elastic protective layer positioned in the window, the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use, wherein the projecting portion is surrounded by dyke formed on a surface of the electronic circuit. However, Nomura et al. (figure 6) teach an elastic material protective layer (132) positioned in the window (127). Nomura et al. inherent teach the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use because a pressure sensitive diaphragm always receives pressure from the top surface of the diaphragm. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate teaching of Nomura et al. into the device taught by Yamawaki et al. because it protects the sensor chip from the external damage. The combined device shows an elastic protective layer positioned in the window, the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use, wherein the projecting portion is surrounded by dyke formed on a surface of the electronic circuit.

Regarding claim 31, Yamawaki et al. (figures 1A-2G) teach a packaged electronic device ready for electronic use, comprising:

a semiconductor integrated electronic circuit (1) having a top, a bottom, and lateral sides extending between the top and bottom;

a plastic protective package (9) in which the electronic circuit (1) is embedded, the protective package (9) supporting the electronic circuit (1) and contacting the lateral sides of the electronic circuit (1), the protective package (9) having a window over a portion of the electronic

circuit (1) such that the electronic circuit (1) can be activated from outside of the protective package (9).

Yamawaki et al. differ from the claimed invention by not showing an elastic protective layer positioned in the window, the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use, wherein the projecting portion is surrounded by dyke formed on a surface of the electronic circuit. However, Nomura et al. (figure 6) teach an elastic material protective layer (132) positioned in the window (127). Nomura et al. inherent teach the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use because a pressure sensitive diaphragm always receives pressure from the top surface of the diaphragm. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate teaching of Nomura et al. into the device taught by Yamawaki et al. because it protects the sensor chip from the external damage. The combined device shows an elastic protective layer positioned in the window, the projecting portion being structured to enable the electronic device to be activated through the projecting portion when the electronic device is in use, wherein the projecting portion is surrounded by dyke formed on a surface of the electronic circuit.

Regarding claim 32, Yamawaki et al. teach the protective package (9) also contacts the top of the electronic circuit (1) adjacent to the window.

Regarding claim 33, the combined device shows the window is defined by tapering walls that taper inwardly toward the electronic circuit (Nomura et al.; 127).

Regarding claim 36, Yamawaki et al. teach the electronic circuit includes a pressure sensor.

Regarding claim 38, the combined device shows the protective layer is shaped to form a ring (Yamawaki et al.; 3) on the electronic circuit (Yamawaki et al.; 1).

6. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,894,707 to Yamawaki et al. in view of US Patent No. 4,823,605 to Stein.

Regarding claim 37, Yamawaki et al. (figure 2f) teach a packaged electronic device ready for electronic use, comprising:

a semiconductor integrated electronic circuit (1) having a top, a bottom, and lateral sides extending between the top and bottom;

a plastic protective package (9) in which the electronic circuit (1) is embedded, the protective package (9) supporting the electronic circuit (1) and contacting the lateral sides of the electronic circuit (1), the protective package (9) having a window over a portion of the electronic circuit (1) such that the electronic circuit (1) can be activated from outside of the protective package (9).

Yamawaki et al. differ from the claimed invention by not showing an elastic protective layer positioned in the window, the protective layer being structured to enable the electronic device to be activated through the protective layer when the electronic device is in use; and a membrane positioned between the electronic circuit and the protective layer, the membrane having a concave surface facing the electronic circuit so as to leave a recess between the concave surface and the electronic circuit. However, Stein (figure 1) teaches an elastic protective layer

(5) positioned in the window (6), the protective layer (5) being structured to enable the electronic device (1) to be activated through the protective layer (5) when the electronic device (5) is in use; and a membrane (4) positioned between the electronic circuit (1) and the protective layer (5), the membrane (4) having a concave surface facing the electronic circuit (1) so as to leave a recess (9) between the concave surface and the electronic circuit (1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stein into the device taught by Yamawaki et al. because it protects the sensor chip form the external damage. The combined device shows an elastic protective layer positioned in the window, the protective layer being structured to enable the electronic device to be activated through the protective layer when the electronic device is in use; and a membrane positioned between the electronic circuit and the protective layer, the membrane having a concave surface facing the electronic circuit so as to leave a recess between the concave surface and the electronic circuit.

Response to Arguments

Applicant's arguments with respect to claims 19, 21, 22, 24, 25, 27-33 and 36-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
May 14, 2004

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